

Analog to Digital IndustryPack Module

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IPM-ADCTM

User Manual

Version 1.0

MAX
technologies

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1 INTRODUCTION

This document describes the capabilities and operation of the IPM-ADC.

The IPM-ADC is a high density, high sampling rate 32MHz single size Industry Pack module. The IPM-ADC incorporates a deep 2048 word FIFO, improving speed and efficiency of the user application. Like all other MAXT products, it also includes a 32-bit 1us timer to accurately time tag all sampling. The module offers many configurable options and features that makes it a perfect choice for many applications.

The module has the following characteristics:

- Single size, 16 bit, 32 MHz IP module with 0 wait state access
- 16-bit ADC converter
- 250kSPS (4us interval)
- High input density of 32 single ended or 16 differential channels (programmable)
- 2048 word deep sampling FIFO concurrent with individual channel sampling value register
- Programmable FIFO interrupt
- Multiple input range: 0-2.5V, 0-5V, 0-10V, +/-2.5V, +/-5V, +/-10V selectable by DIP switch
- Programmable gain: x1, x2, x4, x8
- Per port, individually programmable scan control
- Flexible scanning mode
 - Burst continuous
 - Uniform continuous
- Programmable interval timer (sampling rate)
- External trigger input or output
- 32 bit 1us resolution local timer
- User controllable 1us Sampling Time Tagging
- On board precise calibration voltage
- Programmable output format
- On-board IRIG-B decoder
- +/-15V DC-DC converter for +/-10V range selection without external supply

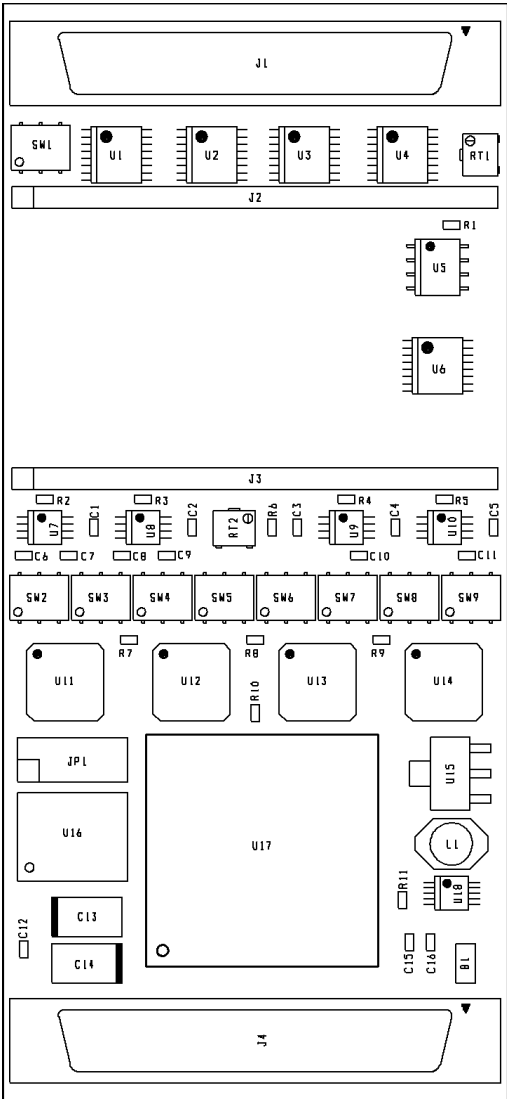


Figure 1-1: IPM-ADC

2 HARDWARE SPECIFICATIONS

The hardware specifications are presented in this section. The following figure presents the block diagram of the IPM-ADC.

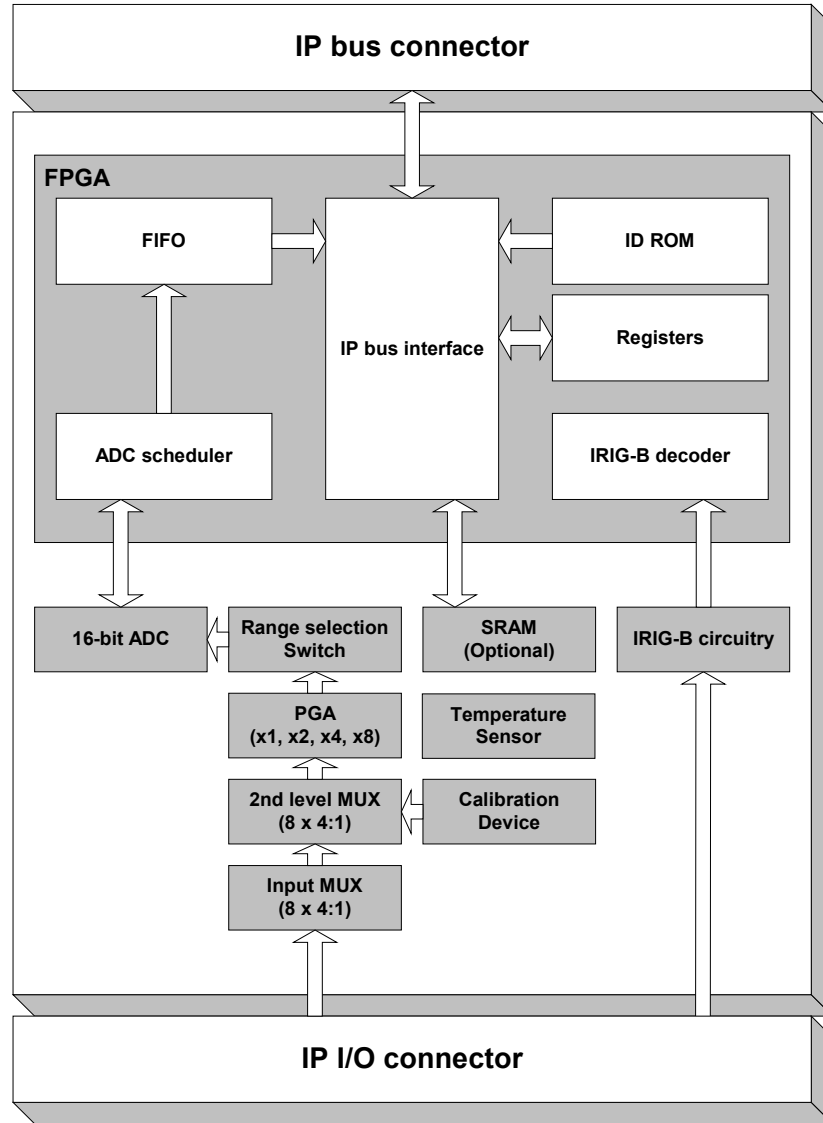


Figure 2-1: IPM-ADC block diagram

2.1 Main Controller (FPGA)

2.1.1 IP bus interface

The host uses this interface to configure the card, read the status, and to transfer the data received. The IO and ID access are done with zero wait state, 62.5 ns, and are compliant with the VITA-4-1995 specification.

2.1.2 ID ROM

Each IP module contains identification data contained in the ID ROM. This section contains information related to the IP; model, revision, active TX and RX, etc... See section 2.7 for mapping.

2.1.3 Registers

The IO registers are used to control all of the functionality of the module. See section 2.8 for detail and mapping.

2.1.4 FIFO

There is one 2048 word deep FIFO on the IPM-ADC, containing data from all enabled channels. A 1us precision time tag can be optionally attached to every data received, or to the first data of a group, which is useful when using the burst mode. The FIFO status is accessible through the FIFO_STATUS register (section 2.9.6), which gives information on the interrupt status, related to almost full threshold and aging time out, overflow status and word count.

Note that the use of the FIFO is optional, the user can also access the sampled data through the ADC_DATA register (address 0x40 through 0x7E). This data is refreshed every time that the channel is sampled. Note that interrupts and timetags are not available through the ADC_DATA register.

2.1.5 ADC scheduler

The ADC scheduler offers three different modes of sampling; burst, uniform and external trigger. When set to burst mode, every enabled channel are scanned as fast as possible each time the interval timer (count down timer, section 2.9.7) gets to zero. The uniform mode will scan one channel per interval timer period. Finally, it is also possible to use the external trigger to initiate the sampling of a channel, thus enabling multiple module simultaneous sampling. Note that the module can also be set to generate the external trigger, in conjunction with the interval timer.

2.1.6 IRIG-B decoder

An IRIG-B decoder on the module can optionally provide IRIG-B time code to user applications and synchronize the IPM-ADC to them for true real-time critical applications. Since the module has a 32bit 1us time tag precision and the IRIG-B time code has a one second resolution, we've implemented an algorithm to precisely correlate the 1us timer to the Pr point of the IRIG-B (start of the time code) or the 1PPS signal if available. (see 2.9.13 IRIGB_SEL Register)

The decoder logic accepts both TTL and standard amplitude-modulated (AM) IRIG-B signals. When using the TTL input, the 1us synchronicity is exact since the rising edge of the TTL output corresponds exactly to the Pr point. When using an AM IRIG-B signal, the decoder circuitry and logic will synchronize on the zero crossing of the beginning of the Pr point of the AM modulated signal. This zero crossing of the low frequency AM modulated signal is not as accurate as the TTL or 1PPS signal. So the user may use a 1PPS signal on the TTL input to improve synchronicity when using the IRIG-B AM signal or compensate. (See application Note: <Calibration process for MAX Technologies product with IRIG.pdf>)

Note that to be able to use the IRIG-B input, the switch SW1 has to be set in the correct position. The double switch gives the possibility to use the corresponding IO as a COMMON, or as an IRIG-B signal (see section 2.3.1 for detail).

Switch #1	POS1	POS2
IO pin 21 connected to:	COMMON	ANALOG IRIG-B

Switch #2	POS1	POS2
IO pin 24 connected to:	COMMON	DIGITAL IRIG-B

Table 2-1: IRIG-B configuration

2.2 16-bit ADC

The analog to digital converter used on the IPM-ADC is the AD7663, a 16-bit charge redistribution SAR converter. The input range is flexible (0-2.5V, 0-5V, 0-10V, +/-2.5V, +/-5V, +/-10V) and can be set with the configuration switch (see section 2.3).

The following table presents the main parameters of the AD7663 converter. See the AD7663 specification for further details.

Parameter	AD7663
Integral Linearity Error	+/-3 LSB max
Signal-to-Noise (100kHz)	90dB
Total Harmonic Distortion (100kHz)	-100dB
-3 dB Input Bandwidth	800kHz
Throughput Rate	250kBPS

Table 2-2: AD7663 specification data

2.3 Range selection switch

The Analog Device AD76xx family devices have multiple input ranges. Changing the input range gives the user the possibility to change the least significant bit value, from 38.15uV for 0-2.5V ranges, to 305.2uV for +/-10V range. See Analog Devices AD76xx specification for detail.

When using the 0-10V and +/-10V ranges, the PGA must be powered by +/-15V. On modules with no DCDC, the user must connect external +/-15V power on the IO connector pin 45/48, and set the jumper JP3 to position 2-3. This will insure correct data conversion over the full +/-10V and 0-10V range. Note that the modules equipped with on board DCDC do not need external power.

The input ranges are selectable through two double switches; the following table presents the switch configuration.

Range	Switch A (SW2/SW4/SW6/SW8)		Switch B (SW3/SW5/SW7/SW9)	
	Switch #1	Switch #2	Switch #1	Switch #2
0-2.5V	POS2	POS2	POS1	Don't care
0-5.0V	POS2	POS2	POS2	POS2
0-10.0V	POS1	POS2	POS2	POS2
+/-2.5V	POS2	POS2	POS2	POS1
+/-5.0V	POS1	POS2	POS2	POS1
+/-10.0V	POS1	POS1	POS2	POS1

Table 2-3: Range selection configuration

Note that the SW2/SW3 are routed to the ADC0, SW4/SW5 are routed to ADC1, SW6/SW7 are routed to ADC2 and SW8/SW9 are routed to ADC3.

2.3.1 Configuration switch

The following figure presents a schematic of the switch that is used for configuration, range selection and IRIG-B. Note that the terminal 1 marking (black dot) can be used to establish the correct switch position on board.



Figure 2-1: Configuration switch

2.4 PGA

The Programmable Gain Amplifier is used to transform the differential input (+ and -), or single ended (+ and sense), into a single ended voltage that is sent to the ADC input. The gain is programmable through IO register GAIN_SELECT (see section 2.10.15), and can be set to x1, x2, x4 or x8. Using the different gain value, in conjunction with the range selection switch gives the user multiple input ranges.

2.5 Calibration device

The calibration device is used to eliminate offset and gain errors that can be created by the input circuitry. High precision voltage values are generated and sent through the PGA to the ADC, and are used for software calibration.

2.6 Input MUX

The input multiplexer features fault-protected inputs and over voltage clamping at 150mV beyond the rails. The fault protection goes up to $\pm 40V$ with supplies off and $\pm 25V$ protection with supplies on. This feature not only protects the modules against higher than $\pm 10V$ input signal, but also protect the tested equipment.

2.7 Single Ended / Differential Input

The IPM-ADC offers the possibility to use single ended and differential input. Although single ended channel can offer very good signal integrity, it is recommended to use differential channels since it offers better noise protection, and therefore more accurate conversions.

When the number of channels that are being sample is lower than 16, the use of differential entry is recommended. The connection of the two polarities of the signals is mandatory, and should be connected to the DXX+ and DXX- of the IO connector.

When a higher number of channels are being sampled (more than 16), the use of single ended entry is necessary. When using single ended entry, the signal reference must be connected to SENSE (IO connector pin 42). The signal itself can than be connected to any of the 32 channels.

Note that it is possible to use some channels as single ended entry, with some other with differential entry. The user must than be very careful to connect the input signals correctly, and set the registers carefully depending on the input connection.

2.8 Temperature sensor

The IPM-ADC is equipped with a temperature sensor, which is place near the FPGA, and gives the possibility to monitor the temperature of the board during operation. Monitoring the temperature of the board is useful when used in conjunction with the calibration voltage; a new set of calibration value should be taken when a temperature drift is detected with the sensor.

The temperature is available with a 0.5°C precision. See register section for detail.

3 MEMORY MAP

3.1 ID ROM region

Address	Description	Value
0x00	ASCII "VI"	0x5649
0x02	ASCII "TA"	0x5441
0x04	ASCII "4 "	0x3420
0x06	Manufacturer ID low 16 bit	0x0000
0x08	Manufacturer ID high 8 bit	0x0000
0x0A	Model #	0x001D
0x0C	Revision #	0x00A1
0x0E	Reserved	0x0000
0x10	Driver ID LSB	0x10E8
0x12	Driver ID MSB	0x0008 => INCLUDED OPTION*
0x14	16-bit flag	0x0004
0x16	No of byte used in the ROM	0x0030
0x18	CRC of the byte used in the ROM	0XXXXX
0x1A	Active TX	0x0000
0x1C	Active RX	0xFFFF
0x1E	Not Used	0x0000
0x20	Not Used	0x0000
0x22	Last Compatible Model	0x0000
0x24	ASCII "IP"	0x4950
0x26	ASCII "MA"	0x4D41
0x28	ASCII "DC"	0x4443
0x2A	ASCII " "	0x2020
0x2C	ASCII " "	0x2020
0x2E	ASCII " "	0x2020

Table 3-1: ID ROM

* : Included option bit definition :

bit 0 : Future use

bit 1 : Future use

bit 2 : Future use

bit 3 : IRIG-B decoder included (Option D)

3.2 IO region

Address	Name	Description	Access
0x00	GLB_CTRL	Control the main functionality: output data format, external trigger, time tag enable, etc...	R/W
0x02	TEMP_SENSOR	Temperature sensor	R
0x04	CH_ENABLE	Channel enable [15..00]	R/W
0x06	CH_ENABLE	Channel enable [31..16]	R/W
0x08	DIFF_ENABLE	Differential channel enable	R/W
0x0A	FIFO_ALFT	FIFO Almost Full Threshold	R/W
0x0C	FIFO_AGTO	FIFO Aging Time Out	R/W
0x0E	FIFO_STATUS	FIFO status	R/W
0x10	INT_TIMER	Conversion interval timer [15..00]	R/W
0x12	INT_TIMER	Conversion interval timer [31..16]	R/W
0x14	FIFO_DATA	Sampling FIFO	R
0x16	IRIG_SEL	IRIG-B register	R/W
0x18	IRIG_TIMER	IRIG-B correlation timer [15..00]	R
0x1A	IRIG_TIMER	IRIG-B correlation timer [31..16]	R
0x1C	IRIG_DATA	IRIG-B data	R
0x1E	IRIG_DATA	IRIG-B data	R
0x20	TT_START	Start Time Tag (1us counter) [15..00]	R/W
0x22	TT_START	Start Time Tag (1us counter) [31..16]	R/W
0x24		Reserved	R/W
0x26		Reserved	R/W
0x28	TIMER	Timer (1us counter) [15..00]	R
0x2A	TIMER	Timer (1us counter) [31..16]	R
0x2C		Reserved	R
0x2E		Reserved	R
0x30-0x3E	GAIN_SELECT	Individual channel gain selection	R/W
0x40-0x7E	ADC_DATA	CH0 – CH31 Received data [15..00] → Channel SE 0x00 or DIFF 0x0	R

Table 3-2: IO registers

3.3 Register Description

3.3.1 GLB_CTRL (0x00)

This register contains the global control, used for every channel.

Bit	Description	Reset	Access
[0]	Global Enable 1 = Global enable 0 = Global disable on end of present cycle	0	R/W
[1]	Start on Time Tag 1 = Indicates to the modules that it must wait until the TT_START = TIMER for acquisition to start after Start Sampling is set to 1.	0	R/W
[3..2]	Time Tag Size X0 = 16-bit time tag X1 = 32-bit time tag	00	R/W
[5..4]	FIFO mode 00 = FIFO disabled 01 = FIFO enabled, no time tag 10 = Time Tag stored for first conversion only 11 = Time Tag stored for each conversion	00	R/W
[6]	FIFO Interrupt Enable 1 = The FIFO generate interrupt on almost full or aging time out	0	R/W
[7]	Not used		
[8]	External Trigger Output Enable 0 = Disable (input), 1 = Enable (Output)	0	R/W
[11..9]	Voltage Calibration 000 = Disabled 001 = 0.000000V 010 = 0.306250V 011 = 0.612500V 100 = 1.225000V 101 = 2.450000V 110 = 4.900000V	000	R/W
[14..12]	Scan Mode 000 = Uniform Continuous 001 = Uniform Single 010 = Burst Continuous 011 = Burst Single 100 = Uniform Continuous on trigger 101 = Uniform Single on trigger 110 = Burst Continuous on trigger 111 = Burst Single on trigger	000	R/W
[15]	Output Data Format 0 = Binary Two's Complement 1 = Straight Binary	0	R/W

3.3.1.1 Global Enable

The Global Enable bit is used to start the sampling on the active channels (see CH_ENABLE register). It should be set to '1' when all of the options are set and the module is ready to start sampling.

3.3.1.2 Start on Time Tag

The Start on Time Tag setting is used in conjunction with Time Tag Start value, and gives the possibility to start the sampling at a 1µs precision time tag. It is useful to set multiple modules to sample at the same time, without the use of External Trigger. When set to '1', the module will not start sampling after the Global Enable is set, it will wait until the Timer value gets to the Time Tag Start value.

3.3.1.3 Time Tag Size

The time tag used in the FIFO can either be set to 16-bit or 32-bit. When set to 16-bit, the time tag read from the FIFO will be the low word.

3.3.1.4 FIFO mode

The FIFO mode gives the possibility to either disable the FIFO, or use it with multiple time tag settings. When disabled, the sampling data can be accessed with the ADC Data registers; there will be no interrupt generation. When enabled, there are three possible settings; no time tag, time tag on first channel sampling, and time tag on every channel conversion. The no time tag setting gives the possibility to minimize the number of access made to the FIFO to retrieve the sampled data. When a time tag is needed, it is possible to generate one for the first channel; the rest of the active channel will not generate time tag in the FIFO. However it is possible to compute the resulting time-tag with the first time tag and the interval timer (ex: TT channel #2 = TT channel #1 + interval timer). Finally, a time tag can be generated of every channel, simplifying external treatment.

3.3.1.5 FIFO interrupt enable

When the FIFO is enabled, interrupt can be generated through IP bus line IRQ0_L. The interrupt enable must be set to '1' to generate those interrupt.

3.3.1.6 External Trigger Output Enable

The external trigger input/output is used to synchronise the sampling with other IPM-ADC module, or with any other source. When set to output ('1'), a 500ns pulse will be outputted when time to scan is reached. When the "on trigger" mode is used (see Scan Mode), the output enable is automatically disabled; the external trigger is used as an input.

3.3.1.7 Voltage calibration

Reference signals for analog input calibration have been provided to improve the accuracy. The use of software calibration allows the elimination of hardware calibration potentiometers traditionally used in precision analog front ends.

Very accurate calibration of the IPM-ADC can be accomplished by using calibration voltages present on the module. The five voltages and the analog ground reference are used to determine two points of a straight line, which defines the analog input characteristic. The calibration voltages are precisely adjusted at the factory to provide optimum performance.

When sampling the calibration value, the user should use a lower rate (uniform sampling at 50kHz) to obtain the highest precision and stability. The calibration value should also be updated periodically to obtain excellent accuracy over temperature changes. Finally, when sampling the calibration data, several reading (recommended 64 to 128) should be taken and averaged to lower as much as possible the measurement uncertainty.

The following equation should be used when software calibration of the ADC data is needed.

$$Corrected_Data = \left[\frac{65536 * m}{Ideal_Voltage_Span} \right] * \left[Sampled_Data + \frac{(Ideal_Cal_Low * Gain) - Ideal_Zero}{m} - Sampled_Cal_Low \right]$$

where:

$$m = Gain * \left[\frac{Ideal_Cal_High - Ideal_Cal_Low}{Sampled_Cal_High - Sampled_Cal_Low} \right]$$

- Gain* = Used PGA gain
- Ideal_Voltage_Span* = See following table
- Ideal_Zero* = See following table
- Ideal_Cal_High* = Ideal value of high calibration voltage
- Ideal_Cal_low* = Ideal value of low calibration voltage
- Sampled_Cal_High* = Measured value of high calibration voltage
- Sampled_Cal_Low* = Measured value of low calibration voltage

Input Range	PGA Gain	Voltage Range	Ideal Cal Low	Ideal Cal High
-2.5 to 2.5	1	-2.5 to 2.5	0	2.45
-2.5 to 2.5	2	-1.25 to 1.25	0	1.225
-2.5 to 2.5	4	-0.625 to 0.625	0	0.6125
-2.5 to 2.5	8	-0.3125 to 0.3125	0	0.30625
-5 to 5	1	-5 to 5	0	4.9
-5 to 5	2	-2.5 to 2.5	0	2.45
-5 to 5	4	-1.25 to 1.25	0	1.225
-5 to 5	8	-0.625 to 0.625	0	0.6125
-10 to 10	1	-10 to 10	0	4.9
-10 to 10	2	-5 to 5	0	4.9
-10 to 10	4	-2.5 to 2.5	0	2.45
-10 to 10	8	-1.25 to 1.25	0	1.225
0 to 2.5	1	0 to 2.5	0.30625	2.45
0 to 5	1	0 to 5	0.30625	4.9
0 to 10	1	0 to 10	0.30625	4.9

Table 3-3: Ideal calibration voltage

Input Range	Ideal Voltage Span	Ideal Zero
-2.5 to 2.5	5.0000	-2.5000
-5 to 5	10.0000	-5.0000
-10 to 10	20.0000	-10.0000
0 to 2.5	2.5000	0.0000
0 to 5	5.0000	0.0000
0 to 10	10.0000	0.0000

Table 3-4: Ideal voltage span and zero

3.3.1.8 Scan Mode

- **Uniform**
The uniform mode (single or continuous) is used to convert every enabled channel, sequentially, at a fix rate; the interval timer register gives the conversion interval between each channels. Therefore, the time taken to convert every channel is given by [Number_of_enabled_channels * Interval_timer].
- **Burst**
The burst mode (single or continuous) is used to convert every enabled channel, sequentially, in a burst sequence. The burst converts every channel at the fastest ADC conversion speed (4us with the AD7663). When set to burst continuous, the burst conversion will be repeated at fix interval; the interval timer register gives the conversion interval between each burst. The time taken to convert every channel is given by [Number_of_enabled_channels * Maximum_ADC_speed].
- **Continuous**
The sampling will start when Global Enable is set to '1', or when Start Time Tag is reached, and will stop when the user set the Global Enable to '0'.
- **Single**
The sampling will start when Global Enable is set to '1', or when Start Time Tag is reached, and will stop when all enabled channels are sampled, the Global Enable automatically goes back to '0'.
- **On trigger**
The on trigger mode sets the module in a slave mode, where burst or uniform conversion will start when a falling edge is detected on the External Trigger pin. Note that Global Enable still must be set to one before any conversion starts.

3.3.1.9 Output data format

The data output format can be programmed to return the ADC data as either Binary 2's complement or straight binary. The following tables present the analog input value related to each of the input voltage range, with the related output code.

Full Scale Range	+/-10V	+/-5V	+/-2.5V	0V to 10V	0V to 5V	0V to 2.5V
LSB	305.2uV	152.6uV	76.3uV	152.6uV	76.3uV	38.15uV
FSR – 1LSB	9.999695V	4.999847V	2.499924V	9.999847V	4.999924V	2.499962V
MID + 1LSB	305.2uV	152.6uV	76.3uV	5.000153V	2.570076V	1.257038V
Midscale (MID)	0V	0V	0V	5V	2.5V	1.25V
MID – 1LSB	-305.2uV	-152.6uV	-76.3uV	4.999847V	2.499924V	1.249962V
– FSR + 1LSB	-9.999695V	-4.999847V	-2.499924V	152.6uV	76.3uV	38.15uV
– FSR	-10V	-5V	-2.5V	0V	0V	0V

Table 3-5: Ideal input voltage

Description	Binary 2's complement	Straight binary
FSR – 1LSB	0x7FFF	0xFFFF
MID + 1LSB	0x0001	0x8001
Midscale (MID)	0x0000	0x8000
0xFFFF	0xFFFF	0xFFFF
– FSR + 1LSB	0x8001	0x0001
– FSR	0x8000	0x0000

Table 3-6: Output code

3.3.2 TEMP_SENSOR (0x02) – Available on Revision B and higher

The module is equipped with a temperature sensor. The value of the sensor is continuously read by the FPGA, and the result is presented in this register. The temperature can have a major impact on the ADC conversion, therefore when high precision measures are needed in a variable temperature system, this register can be monitored, and used to trigger new calibration procedure.

Bit	Description	Reset	Access														
[12..0]	<p>Temperature This value gives the temperature with a precision of 0.5°, from –55 to 128°C.</p> <table border="0"> <tr> <td>127.5°C</td> <td>0111 1111 1111</td> </tr> <tr> <td>...</td> <td>...</td> </tr> <tr> <td>0.5°C</td> <td>0000 0000 0001</td> </tr> <tr> <td>0°C</td> <td>0000 0000 0000</td> </tr> <tr> <td>-0.5°C</td> <td>1111 1111 1111</td> </tr> <tr> <td>...</td> <td>...</td> </tr> <tr> <td>-128°C</td> <td>1000 0000 0000</td> </tr> </table>	127.5°C	0111 1111 1111	0.5°C	0000 0000 0001	0°C	0000 0000 0000	-0.5°C	1111 1111 1111	-128°C	1000 0000 0000	0x000	R
127.5°C	0111 1111 1111																
...	...																
0.5°C	0000 0000 0001																
0°C	0000 0000 0000																
-0.5°C	1111 1111 1111																
...	...																
-128°C	1000 0000 0000																
[14..13]	Not Used	0x0	R														
[15]	<p>Error flag Occurs when the sensor is not responding.</p>	0x0	R														

3.3.3 CH_ENABLE (0x06 - 0x04)

The channel enable register indicates to the module which channel will have to be scanned when global enable is set. This register must be set before setting the global enable bit, it will not be possible to modify when acquisition is active.

The user should be careful when choosing which channel will be enabled. Even though every combination of channels will work, there are performances related with the channels selections. It is recommended to use sequential channel; for example, if only two single ended channels are enabled, it is better to use CH[0] and CH[1], instead of CH[0] and CH[31]. The reason is simple; the FPGA logic looks for the next enabled channel in a sequential way, the faster it finds the next channel, the faster will the MUX stages change, and the more time will the input signal have for settling.

When using channels in differential mode, only channels 0 to 15 are available, channels 16 to 31 becomes the differential pairs. Note that it is possible to use differential settings on some channels, with single ended settings on others simultaneously.

Bit	Description	Reset	Access
[31..0]	<p>Channel Enable 1 = Channel enabled</p>	0x00000000	R/W

3.3.4 DIFF_ENABLE (0x08)

This register is used to set a channel in differential mode; it works in conjunction with the CH_ENABLE (0x06-0x04). The use of differential channel is recommended for the lowest noise and best accuracy.

When a channel from 0 to 15 is enabled, and the matching differential bit is set, the corresponding channel from 16 to 31 is automatically disabled and the pair is working as a differential channel. Note that when a channel from 0 to 15 is disabled, the DIFF_ENABLE is ignored.

Bit	Description	Reset	Access
[15..0]	Differential enable 1 = Differential channel enabled	0x0000	R/W

3.3.5 FIFO_ALFT (0x0A)

This register contains the almost full threshold, in word, used with the FIFO. The almost full threshold is used to generate an interrupt when the number of data in the FIFO gets beyond this level. The FIFO_ALFT is used with the FIFO_STATUS register.

Bit	Description	Reset	Access
[11..0]	FIFO almost full threshold	0x0040	R/W

3.3.6 FIFO_AGTO (0x0C)

This register contains the aging time out, in 512-microsecond accuracy, used with the FIFO. When set to a value different than zero, an interrupt will be generated when data is present in the FIFO longer than (VALUE * 512us). Note that reading or writing in the FIFO resets the aging time out counter. The FIFO_AGTO is used with the FIFO_STATUS register.

Bit	Description	Reset	Access
[6..0]	FIFO aging time-out 0x0000 = disabled	0x0000	R/W

3.3.7 FIFO_STATUS (0x0E)

This register contains the FIFO status. When the FIFO word counter gets to the FIFO_ALFT value, or when data stays in FIFO for FIFO_AGTO * 512us, the status bit will be set to 1. The status bit will go back to '0' as soon as the word count gets under FIFO_ALFT, or, if generated by aging time out, as soon a read is made to the FIFO. Note that writing a '1' to the status bit will clear the FIFO, and it is highly recommended to disable the Global Enable before clearing the FIFO.

In the case where the FIFO gets full, and an overflow occurs, there will be no new data written in the FIFO until the user begins to read. However, even if the data integrity is preserved on an overflow, the user must disable the conversion, clear the FIFO, and start back the conversion to be able to continue, since once an overflow occurs, there is no way to know how much data where lost, therefore the data synchronization is lost. An overflow will generate an IP_ERROR_L and will set the corresponding flag to '1', the flag must be cleared by writing a '1' to it.

The word count can be used in conjunction with the interrupt status bit. When the host receives an interrupt, the word count is read, and the number of data available is read from the FIFO. Doing this will improve performance, since the number of data in the FIFO can change between the time the interrupt is issued, and the time the host services it.

Bit	Description	Reset	Access
[15]	Overflow Write '1' to clear Overflow flag	0	R/W*
[14]	Interrupt status Write '1' to reset FIFO	0	R/W*
[13]	Unused	0	R
[12..0]	Word count Indicates the number of words present in the FIFO (max 2048). For extended FIFO, the word count will top at 2048, and will stay there until the real word count goes under this value.	0x0000	R

3.3.8 INT_TIMER (0x10 - 0x12)

This register contains the interval timer used to compute the sampling rate. The value, in microsecond, represents the time between sampling, either in burst or uniform mode. Note that the value should be set before the Global Enable is set, but it is possible to modify the interval timer when the conversion is running.

Bit	Description	Reset	Access
[31..0]	Interval timer Value, in microsecond, of the interval time between conversions.	0x00000000	R/W

When set to burst mode, the interval timer represent the time between the last sample of a burst, and the first sample of the next burst. The following figure represents the two sampling mode.

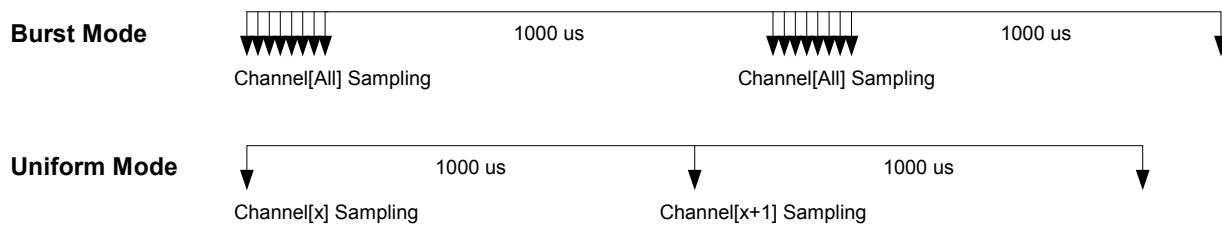


Figure 3-1: Interval timer

The smallest sampling interval depends on the type of ADC used, and on the number of channel selected; it is represented by the following equation:

$$\text{Smallest Sampling Interval (sec)} = \text{Number of Channel} * (1 / \text{ADC speed (SPS)})$$

In this equation, when using the uniform mode, the number of channel is 1. Note that if the value set in the register is smaller than this value, the sampling rate will peak at the smallest sampling interval value.

3.3.9 FIFO_DATA (0x14)

The data FIFO is used as a buffer between the ADC and the carrier card. When enabled, the FIFO will contain the sampled data of every channel enabled, with the corresponding time tag, see GLB_CTRL register for detail. The maximum number of word that can be contained in the FIFO is 2048.

The user should always make sure that the FIFO is empty before setting the Global Enable (not that after a card reset, the FIFO is always empty). This must be done since there will be no way to correctly recover the data if the FIFO is not empty at the start of a conversion sequence.

Although the read order is always time tag followed by data, the following table present the different configuration, and their impact on the FIFO access.

Number of ADC	FIFO mode	Read order
1	Time tag on all	- Time tag CH0 * - Data CH0 - Time tag CH1 - Data CH1 - ...
	Time tag on first	- Time tag CH0 - Data CH0 - Data CH1 - Data CH2 - ...
	No time tag	- Data CH0 - Data CH1 - Data CH2 - ...
4	Time tag on all	- Time tag CH0 - Data CH0 - Data CH1 - Data CH2 - Data CH3 - Time tag CH4 - Data CH5 - Data CH6 - ...
	Time tag on first	- Same as with 1 ADC
	No time tag	- Same as with 1 ADC

* Time tag can be 16-bit or 32-bit, when 32-bit is used, the high word is accessed first.

3.3.10 IRIGB_SEL (0x16)

The IRIGB_TTL_EN gives the possibility to use the TTL entry. When TTL enabled, the IRIGB_TTL_CONFIG is used to choose between an IRIG-B digital input and a 1PPS digital input, which is a 1 Hz TTL signal, with the rising edge precisely on the IRIG second (used in conjunction with the AM IRIG-B signal). When the IRIG-B digital input is used, the AM IRIG-B input is ignored. (See application note: <Q&A IRIG-B correlation.pdf> for more details on how to correlate Time Tag with IRIG-B Time code)

Note that to use the IRIG-B functionality, the jumpers of J8 must be set on pins 4-6 and pins 3-5. When this is done the IO23+ and the IO23- cannot be used.

Bit	Name	Description	Reset value
0..13	Reserved		0
14	IRIGB_TTL_EN	When set to one, the DIO6 is used as a TTL IRIG-B signal. 1 => IRIG-B TTL enable	0
15	IRIGB_TTL_CONFIG	Gives the option between IRIG-B TTL entry or 1PPS signal used in correlation with IRIG-B AM signal. 0 => IRIG-B TTL digital 1 => IRIG-B 1PPS signal	0

3.3.11 IRIG_CTT (0x18 - 0x1A)

When the IRIG-B is enabled, IRIG_CTT is used as a correlation time-tag with the IRIG-B time. When the IRIG-B second is reached, the internal 32-bit microsecond timer is latched, which gives the correlation between the IRIG-B time and microsecond time. In that case, when reading the IRIG_CTT LSB (0x18), the IRIG_CTT MSB and the IRIG_DATA are latched, and will only be latched again after the IRIG_DATA is accessed.

Bit	Description	Reset	Access
[31..0]	IRIG_CTT	0x00000000	R

3.3.12 IRIGB_DATA (0x1C - 0x1E)

This register shows the last set of information the IRIG-B decoder has captured. If no IRIG-B signal is fed to the decoder circuitry, these registers will remain at their reset value. The following table describes the content of the registers (bits 16 to 31 represent bits 0 to 15 of the second register); the IRIG_DATA LSB must always be read first, followed by the MSB. These registers are read-only. Note: IRIG-B signals often give Greenwich Mean Time (GMT+00:00).

Bit	Description	Reset value
0-3	Units of seconds	0000
6-4	Tens of seconds	000
10-7	Units of minutes	0000
13-11	Tens of minutes	000
17-14	Units of hours	0000
19-18	Tens of hours	00
23-20	Units of days	0000
27-24	Tens of days	0000
29-28	Hundreds of days	00

3.3.13 TT_START (0x20 - 0x22)

This register contains the time tag start value, in microsecond; it is used in conjunction with the Start on Time Tag bit in the GLB_CTRL register. The acquisition will start when the TIMER gets to TT_START value, after the Global Enable is set.

As mentioned previously, this option is useful to synchronize multiple modules without the use of the external trigger signal. To do so, the same TT_START must be set, along with the same INT_TIMER on every module, before setting the Global Enable.

Bit	Description	Reset	Access
[31..0]	TT_START Value, in microsecond, of the start time	0x00000000	R/W

3.3.14 TIMER (0x28 - 0x2A)

This register contains the microsecond precision timer. The value is reset when IP_STROBE_L is detected, and the TIMER MSB is latched when the TIMER LSB is accessed.

Bit	Description	Reset	Access
[31..0]	TIMER	0x00000000	R

3.3.15 GAIN_SELECT (0x30-0x3E)

The gain select registers give the possibility to select a different gain for every channel. The gain must be chosen depending on the type of signal that will be sampled on the channel. For example, if the input range is set to +/-5V, and the input signal is known to be a +/-1V signal, a gain of 4 could be apply to the input, so the ADC range (with gain of 4, +/-1.25V) would be more adapted to the signal.

Bit	Description	Reset	Access
[15..0]	GAIN_SELECT [15..12] → Channel SE 0x03 [11..08] → Channel SE 0x02 or DIFF 0x1 [07..04] → Channel SE 0x01 [03..00] → Channel SE 0x00 or DIFF 0x0 Where: XX00 → Gain of 1 XX01 → Gain of 2 XX10 → Gain of 4 XX11 → Gain of 8	0x0000	R/W

3.3.16 ADC_DATA (0x40-0x7E)

When a channel is scanned, the value is latched into the corresponding register. Those register work independently of FIFO, or scanning mode. The ADC_DATA register is useful when the use of interrupt is not relevant to the application, and a pooling approach is preferred.

Bit	Description	Reset	Access
[15..0]	ADC_DATA	0x0000	R

4 THE IO CONNECTOR PIN DEFINITION

The IO connector pin-out is given in the following table:

Pin #	Function
1	SE00, D00+
2	SE16, D00-
3	COMMON
4	SE01, D01+
5	SE17, D01-
6	COMMON
7	SE02, D02+
8	SE18, D02-
9	COMMON
10	SE03, D03+
11	SE19, D03-
12	COMMON
13	SE04, D04+
14	SE20, D04-
15	COMMON
16	SE05, D05+
17	SE21, D05-
18	COMMON
19	SE06, D06+
20	SE22, D06-
21	COMMON / ANALOG IRIG-B
22	SE07, D07+
23	SE23, D07-
24	COMMON / DIGITAL IRIG-B
25	SE08, D08+
26	SE24, D08-
27	COMMON
28	SE09, D09+
29	SE25, D09-
30	COMMON
31	SE10, D10+
32	SE26, D10-
33	COMMON
34	SE11, D11+
35	SE27, D11-
36	COMMON
37	SE12, D12+
38	SE28, D12-
39	COMMON
40	SE13, D13+
41	SE29, D13-
42	SENSE
43	SE14, D14+
44	SE30, D14-
45	+15V (not used)
46	SE15, D15+
47	SE31, D15-
48	-15V (not used)
49	EXT TRIG
50	SHIELD

Table 4-1: IP IO Connector definition

5 SPECIFICATIONS

5.1 General Specifications

ADC:	Analog Devices AD7663
A/D Resolution	16-bit
Data Format	Binary 2's Complement and Straight Binary
A/D Integral Linearity	3 LSB max
Unipolar Zero Error	+/- 0.18% of Full Scale Range
Bipolar Zero Error	+/- 0.06% of Full Scale Range
Unipolar Full-Scale Error	+/- 0.38% of Full Scale Range
Bipolar Full-Scale Error	+/- 0.25% of Full Scale Range
PGA (1ADC version):	Burr-Brown (TI) PGA206
PGA Linearity Error	0.005% max
Gain Error	0.01% Typical, 0.1% max
Analog Input	
Input Resistance	10E10 Ohms
Input Over voltage Protection	±40V Fault Protection with Power Off ±25V Fault Protection with Power On

5.2 Physical specifications

IPM-ADC is fully compliant to the Industry Pack module single size type II mechanical specification. See VITA 4-1995 Draft 1.0.d.0 April 7, 1995

5.3 Environmental Specifications

Operational temperature	0°C to 70°C (regular version) -40°C to 85°C (extended temperature version)
Relative Humidity	0-95%
Storage temperature	-55°C to 125°C

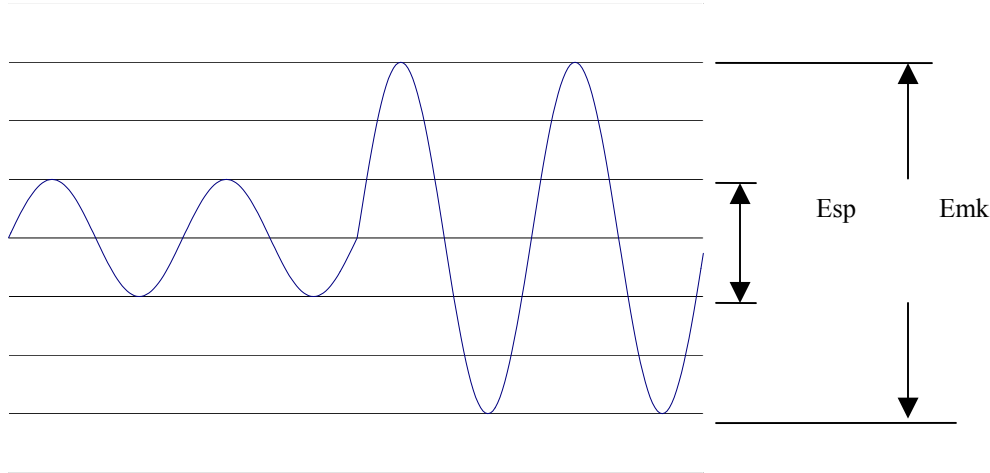
5.4 Power Specifications

IPM-ADC – Basic	
+5V	40mA
+12V	25mA
-12V	25mA
IPM-ADC – +/-15V DCDC	
+5V	233mA
+12V	10mA
-12V	10mA

Maximum value, tested during 32-channel sampling, burst mode.

APPENDIX A

IRIG-B AM input signal requirement



Esp : Space Amplitude : MINIMUM amplitude = 0.5V peak to peak
 Emk : Mark Amplitude : MAXIMUM amplitude = 10V peak to peak

Mark to Space RATIO (Emk / Esp) = 2.5:1 and up

IRIG supported format combination:

IRIG-B 122 & IRIG-B 002 where:

Format:	Modulation Frequency:	Frequency/ Resolution:	Coded Expression:
B	1 (Sine wave, amplitude modulated - AM)	2 (1kHz/1ms)	2 (BCD)*
B	0 (Pulse width code – TTL)	0 (No carrier)	2 (BCD)*

*: 0 (BCD,CF,SBS), 1 (BCD,CF) & 3 (BCD,SBS) coded expressions are also supported, but only the BCD part will be decoded.